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NAVAL RESEARCH LABORATORY
ASSOCIATE COUNSEL (PATENTS)
CODE 1008.2
4555 OVERLOOK AVENUE, S.W.
WASHINGTON, DC 20375-5320

EXAMINER	
KING, JUSTIN	

ART UNIT	PAPER NUMBER
2111	

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17

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/715,772	Applicant(s) DENNIS ET AL.	
	Examiner Justin I. King	Art Unit 2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *40* is/are allowed.

6)☒ Claim(s) *1-39 and 41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. In view of the Appeal Brief filed on 8/26/04, PROSECUTION IS HEREBY REOPENED. New grounds of Rejections are set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) request reinstatement of the appeal.

If reinstatement of the appeal is requested, such request must be accompanied by a supplemental appeal brief, but no new amendments, affidavits (37 CFR 1.130, 1.131 or 1.132) or other evidence are permitted. See 37 CFR 1.193(b)(2).

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-12, 14-25, 27-38, and 41 are rejected under 35 U.S.C. 102(b) as being anticipated by Motomura (U.S. Patent No. 5,815,727).

Referring to claim 1: Motomura discloses a processing slice (figure 1, structure 100) to execute a plurality of threads. Motomura's processing slice comprises a functioning unit (figure 1, structure 110) to perform a register operation (column 8, lines 1-51). The requestor/generator for the threaded operations is the peripheral device, and the means to convey the request is the peripheral bus.

As stated by both the Application Specification and the previous response Paper #13, each processing slice executes several instructions concurrently in the same clock cycle by interleaving the instructions' fetch, decode, dispatch, and execution (Paper#13, page 2, lines 6-7, Specification, page 8, lines 21-25). Motomura discloses forking other threads during execution of a certain thread (column 8, lines 15-27), which is the claimed execution, fetch, and decode in the same clock cycle.

As stated by both the Application Specification and previous response Paper #13, the claimed limitation "functional unit to perform a register operation specified in the instructions in each of the plurality of threads" directs toward performing an operation specified in the dispatched instruction and performs all operations of the instruction set that manipulate values in the data registers (Paper#13, page 2, lines 8-10, Specification, page 12, lines 5-7). Motomura discloses performing operations dispatched via the bus 111 (column 8, lines 15-23); thus, Motomura discloses that the functional unit performs a register operation specified in the instructions in each of the plurality of threads

Hence, claim is anticipated by Motomura.

Referring to claims 2-3: Any request from the user, such as keyboard inputs or printing, trigs a threaded operation. Such request is an I/O operation, and the device receives the request, such as a keyboard or a mouse, is an I/O device.

Referring to claim 4: Motomura discloses the message content (column 8, lines 36-39).

Referring to claim 5: Once each thread's program counter finishes every associated instruction and is ready for a new thread, the means to ask for new thread's information indicates the completion of the previous thread.

Referring to claim 6: Motomura discloses the processing parameters and the pointer pointing to the parameters (column 8, lines 37-38). The pointer is the data register address.

Referring to claim 7: Motomura's bus is bi-directional (figure 1, structures 111 and 112, column 8, line 16).

Referring to claims 8-9: Motomura discloses executing a different thread while the first thread is in a waiting state (column 8, lines 40-42). Motomura's switching to different thread is the claimed disabling the first thread. Motomura discloses an executing scenario which executing a program sequentially without dividing (column 1, line 61). The disclosed executing a program without dividing is the claimed continuing to execute if in a non-wait instruction.

Referring to claim 10: Motomura discloses resuming the thread previously in a waiting state (column 2, lines 59-60).

Referring to claim 11: Motomura discloses an instruction processing unit (figure 1, structure 150) to process instructions fetched from a program memory (figure 1, structure 140); and a thread control unit (figure 16's thread execution control system) coupled to the instruction processing unit to manage initiating and termination of at least one of the plurality of threads.

Referring to claim 12: Motomura discloses a memory access unit (figure 16, structure 620) coupled to the instruction processing unit to provide access to one of a plurality of data memories (figure 5, structure 541) via a data memory switch (figure 5, structure 542), the memory access unit having a plurality of data base registers (figure 16, structure 1610), each of the data base registers corresponding to each of the threads; and a functional unit (figure 1, structure 110) coupled to the instruction processing unit to perform an operation specified in one of the instructions; and a register file (figure 16, structure 1420) having a plurality of data registers (figure 16, structure 1410), each of the data registers corresponding to each of the threads.

Referring to claim 14: Motomura discloses a processing slice (figure 1, structure 100) to execute a plurality of threads. Motomura's processing slice comprises functioning unit (figure 1, structure 110) to perform a register operation (column 8, lines 1-51). The requestor/generator for the threaded operations is the peripheral device, and the means to convey the request is the peripheral bus.

As stated by both the Application Specification and the previous response Paper #13, each processing slice executes several instructions concurrently in the same clock cycle by interleaving the instructions' fetch, decode, dispatch, and execution (Paper#13, page 2, lines 6-7, Specification, page 8, lines 21-25). Motomura discloses forking other threads during execution of a certain thread (column 8, lines 15-27), which is the claimed execution, fetch, and decode in the same clock cycle.

As stated by both the Application Specification and previous response Paper #13, the claimed limitation "functional unit to perform a register operation specified in the instructions in

each of the plurality of threads" directs toward performing an operation specified in the dispatched instruction and performs all operations of the instruction set that manipulate values in the data registers (Paper#13, page 2, lines 8-10, Specification, page 12, lines 5-7). Motomura discloses performing operations dispatched via the bus 111 (column 8, lines 15-23); thus, Motomura discloses that the functional unit performs a register operation specified in the instructions in each of the plurality of threads

Hence, claim is anticipated by Motomura.

Referring to claims 15-16: Any request from the user, such as keyboard input or printing, trigs a threaded operation. Such request is an I/O operation, and the device receives the request, such as a keyboard or a mouse, is an I/O device.

Referring to claim 17: Motomura discloses the message content (column 8, lines 36-39).

Referring to claim 18: Once each thread's program counter finishes every associated instruction and is ready for a new thread, the means to ask for new thread's information indicates the completion of the previous thread.

Referring to claim 19: Motomura discloses the processing parameters and the pointer pointing to the parameters (column 8, lines 37-38). The pointer is the data register address.

Referring to claim 20: Motomura's bus is bi-directional (figure 1, structures 111 and 112, column 8, line 16).

Referring to claims 21-22: Motomura discloses executing a different thread while the first thread is in a waiting state (column 8, lines 40-42). Motomura's switching to different thread is the claimed disabling the first thread. Motomura discloses an executing scenario which

executing a program sequentially without dividing (column 1, line 61). The disclosed executing a program without dividing is the claimed continuing to execute if in a non-wait instruction.

Referring to claim 23: Motomura discloses resuming the thread previously in a waiting state (column 2, lines 59-60).

Referring to claim 24: Motomura discloses an instruction processing unit (figure 1, structure 150) to process instructions fetched from a program memory (figure 1, structure 140); and a thread control unit (figure 16's thread execution control system) coupled to the instruction processing unit to manage initiating and termination of at least one of the plurality of threads.

Referring to claim 25: Motomura discloses a memory access unit (figure 16, structure 620) coupled to the instruction processing unit to provide access to one of a plurality of data memories (figure 5, structure 541) via a data memory switch (figure 5, structure 542), the memory access unit having a plurality of data base registers (figure 16, structure 1610), each of the data base registers corresponding to each of the threads; and a functional unit (figure 1, structure 110) coupled to the instruction processing unit to perform an operation specified in one of the instructions; and a register file (figure 16, structure 1420) having a plurality of data registers (figure 16, structure 1410), each of the data registers corresponding to each of the threads.

Referring to claim 27: Motomura discloses a plurality of data memories (figure 5, structure 541), a memory switch (figure 16, structure 620), and program memory (figure 16, structure 1610). Motomura discloses a processing slice (figure 1, structure 100) to execute a plurality of threads. Motomura's processing slice comprises functioning unit (figure 1, structure 110) to perform a register operation (column 8, lines 1-51). The requestor/generator for the

threaded operations is the peripheral device, and the means to convey the request is the peripheral bus.

As stated by both the Application Specification and the previous response Paper #13, each processing slice executes several instructions concurrently in the same clock cycle by interleaving the instructions' fetch, decode, dispatch, and execution (Paper#13, page 2, lines 6-7, Specification, page 8, lines 21-25). Motomura discloses forking other threads during execution of a certain thread (column 8, lines 15-27), which is the claimed execution, fetch, and decode in the same clock cycle.

As stated by both the Application Specification and previous response Paper #13, the claimed limitation "functional unit to perform a register operation specified in the instructions in each of the plurality of threads" directs toward performing an operation specified in the dispatched instruction and performs all operations of the instruction set that manipulate values in the data registers (Paper#13, page 2, lines 8-10, Specification, page 12, lines 5-7). Motomura discloses performing operations dispatched via the bus 111 (column 8, lines 15-23); thus, Motomura discloses that the functional unit performs a register operation specified in the instructions in each of the plurality of threads

Hence, claim is anticipated by Motomura.

Referring to claims 28-29: Any request from the user, such as keyboard input or printing, trigs a threaded operation. Such request is an I/O operation, and the device receives the request, such as a keyboard or a mouse, is an I/O device.

Referring to claim 30: Motomura discloses the message content (column 8, lines 36-39).

Referring to claim 31: Once each thread's program counter finishes every associated instruction and is ready for a new thread, the means to ask for new thread's information indicates the completion of the previous thread.

Referring to claim 32: Motomura discloses the processing parameters and the pointer pointing to the parameters (column 8, lines 37-38). The pointer is the data register address.

Referring to claim 33: Motomura's bus is bi-directional (figure 1, structures 111 and 112, column 8, line 16).

Referring to claims 34-35: Motomura discloses executing a different thread while the first thread is in a waiting state (column 8, lines 40-42). Motomura's switching to different thread is the claimed disabling the first thread. Motomura discloses an executing scenario which executing a program sequentially without dividing (column 1, line 61). The disclosed executing a program without dividing is the claimed continuing to execute if in a non-wait instruction.

Referring to claim 36: Motomura discloses resuming the thread previously in a waiting state (column 2, lines 59-60).

Referring to claim 37: Motomura discloses an instruction processing unit (figure 1, structure 150) to process instructions fetched from a program memory (figure 1, structure 140); and a thread control unit (figure 16's thread execution control system) coupled to the instruction processing unit to manage initiating and termination of at least one of the plurality of threads.

Referring to claim 38: Motomura discloses a memory access unit (figure 16, structure 620) coupled to the instruction processing unit to provide access to one of a plurality of data memories (figure 5, structure 541) via a data memory switch (figure 5, structure 542), the memory access unit having a plurality of data base registers (figure 16, structure 1610), each of

the data base registers corresponding to each of the threads; and a functional unit (figure 1, structure 110) coupled to the instruction processing unit to perform an operation specified in one of the instructions; and a register file (figure 16, structure 1420) having a plurality of data registers (figure 16, structure 1410), each of the data registers corresponding to each of the threads.

Referring to claim 41: Motomura discloses a multi-thread processor (figure 1, structure 100) having program registers (figure 16, structure 1410) and data base registers (figure 16, structure 1610). Motomura discloses a processing slice (figure 1, combined structures 120, 111, 112, and 110) to execute a plurality of threads. Motomura's processing slice comprises a functioning unit (figure 1, structure 110) to perform a register operation (column 8, lines 1-51). The requestor/generator for the threaded operations is the peripheral device, and the means to convey the request is the peripheral bus.

As stated by both the Application Specification and the previous response Paper #13, each processing slice executes several instructions concurrently in the same clock cycle by interleaving the instructions' fetch, decode, dispatch, and execution (Paper#13, page 2, lines 6-7, Specification, page 8, lines 21-25). Motomura discloses forking other threads during execution of a certain thread (column 8, lines 15-27), which is the claimed execution, fetch, and decode in the same clock cycle.

As stated by both the Application Specification and previous response Paper #13, the claimed limitation "functional unit to perform a register operation specified in the instructions in each of the plurality of threads" directs toward performing an operation specified in the dispatched instruction and performs all operations of the instruction set that manipulate values in

the data registers (Paper#13, page 2, lines 8-10, Specification, page 12, lines 5-7). Motomura discloses performing operations dispatched via the bus 111 (column 8, lines 15-23); thus, Motomura discloses that the functional unit performs a register operation specified in the instructions in each of the plurality of threads.

Hence, claim is anticipated by Motomura.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claims 13, 26, and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of the Motomura and Hiraoka et al. (U.S. Patent No. 5,418,917).

Referring to claims 13, 26, and 39: Motomura discloses an instruction fetch unit (figure 5, structure 150) to fetch the instructions from the program memory using a plurality of program counters (figure 15, structure 140), each program counter corresponding to each of the threads;

an instruction decoder (figure 5, structure 542) and dispatcher (figure 5, structure 150) to decode the instructions and dispatch the decoded instructions to one of the memory access unit, the functional unit, and the peripheral unit. Motomura does not explicitly disclose a buffer to hold the fetched instructions.

Hiraoka discloses that the instruction buffer is a well-known industrial practice to pipelining the processing requests (figure 1). Hence, it would be obvious to one having ordinary skill in the computer art at time Applicant made the invention to adapt Hiraoka's instruction buffer onto Motomura because Hiraoka teaches one to further enhance system performance with an instruction buffer.

7. Claim 40 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of the Motomura and Dove et al. (U.S. Patent No. 5,938,765).

Referring to claim 40: Motomura discloses a multi-thread processor (figure 1, structure 100). Motomura discloses a processing slice (figure 1, combined structures 120, 111, 112, and 110) to execute a plurality of threads. Motomura's processing slice comprises functioning unit (figure 1, structure 110) to perform a register operation (column 8, lines 1-51). The requestor/generator for the threaded operations is the peripheral device, and the means to convey the request is the peripheral bus.

As stated by both the Application Specification and the previous response Paper #13, each processing slice executes several instructions concurrently in the same clock cycle by interleaving the instructions' fetch, decode, dispatch, and execution (Paper#13, page 2, lines 6-7, Specification, page 8, lines 21-25). Motomura discloses forking other threads during execution

of a certain thread (column 8, lines 15-27), which is the claimed execution, fetch, and decode in the same clock cycle.

As stated by both the Application Specification and previous response Paper #13, the claimed limitation "functional unit to perform a register operation specified in the instructions in each of the plurality of threads" directs toward performing an operation specified in the dispatched instruction and performs all operations of the instruction set that manipulate values in the data registers (Paper#13, page 2, lines 8-10, Specification, page 12, lines 5-7). Motomura discloses performing operations dispatched via the bus 111 (column 8, lines 15-23); thus, Motomura discloses that the functional unit performs a register operation specified in the instructions in each of the plurality of threads.

Motomura only discloses a multi-thread processor (figure 1, structure 100), Motomura does not discloses a plurality of the multi-thread processors. Dove discloses a computer system with a node structure (figure 1). Each of Dove's nodes includes a plurality of processors (figure 1), which enables each node to concurrently process a plurality of threads. Thus, each of Dove's nodes is equivalent to a multi-thread processor, and Dove teaches one to increase the system processing power with the multi-node architecture. Hence, it would have been obvious to one having ordinary skill in the computer art to adopt Dove's teaching onto Motomura because Dove teaches one the multi-node architecture to further increase the system processing power.

Response to Arguments

8. Applicant states that the processing slice is able to dispatch instructions to any of the functional units within the processing unit (Paper#13, page 3, lines 6-7). The specification does not disclose a processing slice with a plurality of processing units.

Conclusion

9. **THIS ACTION IS MADE NON-FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Justin I. King whose telephone number is 571-272-3628. The examiner can normally be reached on Monday through Friday, 9:00 am to 5:00 pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 571-272-3632 or on the central telephone number, (571) 272-2100. The fax

phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lastly, paper copies of cited U.S. patents and U.S. patent application publications will cease to be mailed to applicants with Office actions as of June 2004. Paper copies of foreign patents and non-patent literature will continue to be included with office actions. These cited U.S. patents and patent application publications are available for download via the Office's PAIR. As an alternate source, all U.S. patents and patent application publications are available on the USPTO web site (www.uspto.gov), from the Office of Public Records and from commercial sources. Applicants are referred to the Electronic Business Center (EBC) at http://www.uspto.gov/ebc/index.html or 1-866-217-9197 for information on this policy. Requests to restart a period for response due to a missing U.S. patent or patent application publications will not be granted.

MARK H. RINEHART
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

Justin King
December 11, 2004